

## **POWER ESTIMATION AND OPTIMIZATION METHODOLOGIES FOR VLIW BASED EMBEDDED SYSTEMS%0A**

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Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems by Vittorio Zaccaria Politecnico di Milano, Italy Mariagiovanna Sami Politecnico di Milano, Italy  
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### **POWER ESTIMATION AND VLIW BASED EMBEDDED SYSTEMS**

innovative power estimation and optimization methodologies to support the design of low power embedded systems based on high-performance Very Long Instruction Word (VLIW) microprocessors.  
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### **Power Estimation and Optimization Methodologies for VLIW**

This book is entirely devoted to disseminate the results of a long term research program between Politecnico di Milano (Italy) and STMic- electronics, in the field of architectural exploration and optimization techniques to designing low power embedded systems.  
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### **Power Estimation and Optimization Methodologies for VLIW**

LOW power design is playing an important role in today ultra-large scale integration (ULSI) design, particularly as we continue to double the number of transistors on a die every two years and increase the frequency of operation at fairly the same rate. Certainly, an important aspect of low power  
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### **An instruction level methodology for power estimation and**

An instruction-level methodology for power estimation and optimization of embedded VLIW cores  
Abstract: Summary form only given. The overall goal of this work is to define an instruction-level power macro-modeling and characterization methodology for VLIW embedded processor cores.  
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### **Power estimation and optimization for VLIW based embedded**

Power estimation and optimization for VLIW-based embedded systems; Vittorio Zaccaria, Stojcev, Mile 2004-04-01 00:00:00 Microprocessors have been designed for about forty years. Within that period their performance has seen a tremendous increase.

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### **Energy estimation and optimization of embedded VLIW**

In this paper, we propose a system-level power exploration methodology for embedded VLIW architectures based on an instruction-level analysis. The instruction-level energy model targets a general

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### **Part I Power Estimation Methods Engineering360**

In this chapter we present the main sources of power consumption in digital VLSI circuits based on static CMOS technology. In particular, we briefly analyze the main parameters affecting the total power consumption, namely the clock frequency, the supply voltage, the capacitive load, and the switching activity.

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