

## REUSE METHODOLOGY MANUAL FOR SYSTEM ON A CHIP DESIGNS%0A

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### **Reuse Methodology Manual for System on a Chip Designs**

reuse methodology manual for system -on-a-chip designs third edition By Michael Keating Synopsys, Inc. Pierre Bricaud Synopsys, Inc. KLUWER ACADEMIC PUBLISHERS NEW YORK, BOSTON, DORDRECHT, LONDON, MOSCOW

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### **Reuse Methodology Manual for System on a Chip Designs**

Design reuse - the use of pre-designed and pre-verified cores - is the most promising opportunity to bridge the gap between available gate-count and designer productivity. Reuse Methodology Manual for System-On-A-Chip Designs outlines an effective methodology for creating reusable designs for use in a System-on-a-Chip (SoC) design methodology.

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Silicon technology now allows us to build chips consisting of tens of millions of transistors. This technology not only promises new levels of system integration onto a single chip, but also presents significant challenges to the chip designer.

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The release adds support for Reuse Methodology Manual (RMM) design rules that define a methodology for efficient reuse and verification of System-On-A-Chip (SoC) designs.

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